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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,653	07/22/2002	Richard Spitz	10191/2277	9239

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,653	SPITZ, RICHARD	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/2/4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The examiner has included a signed copy of Form PTO-892with the present Office Action. All items thereon had previously been considered and are being considered.

Response to Amendment

Amendment filed 2/2/4 forms the basis of this Office Action. In said Amendment Applicant has substantially amended all claims through substantial amendment of the independent claims 9 and 16. Claims 1-8 have previously been cancelled. Claims 9-16 are in the application. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Response to Arguments

1. Applicant's arguments filed 2/2/4 have been fully considered but they are not persuasive. In particular, with regard to the statement by Applicant that "Henry does not teach that the layers of a semiconductor component only have depressions in an internal area and do not have depressions in edge areas" is true but said teaching is obvious in view of Goodrich et al (5,343,070). Aforementioned statement has only been included in the claim language through said Amendment. The following claim rejections are offered at the earliest possible time.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 16*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al (FR 75-24147 (Application Number)) in view of Goodrich et al (5,343,070).

Henry et al teach a semiconductor component (cf. title and page 1, l. 1-10) comprising: a first layer 2 (cf. page 2, l. 26-30 and page 4, l. 5-7, from the latter it is evident that p- is an alternative to I type for region 2) of a first conductivity type (lightly doped, p- type) having a top side and a bottom side, the first layer having areas of different thickness due to at least one depression 111 (and 112 cf. page 3, l. 6-14) introduced into the top side; a second layer 3 (cf. page 2, l. 26-30) of a second conductivity type (n+ type) covering the top side of the first layer; and a third layer 1 situated on the bottom of the first layer (cf. page 2, l. 26-30), wherein the first, second and third layers are diced into individual chips (along 21 and 23) (cf. Figure 1) (cf. page 2, l. 22-30), so that, in an internal area, each of the chips has at least one depression 111 or 112, and wherein the depression is sawed (cf. page 1, l. 36 – page 2, l. 3).

Henry et al do not necessarily teach the limitation that said depression to be sawed in an internal area such that none of the first layer, second layer and third layer include edge areas that have depressions. *However, it would have been obvious* to

include said limitation in view of Goodrich et al, who teach a mesa type PIN diode (cf. title) and a method of making mesa type PIN diodes (cf. abstract) wherein the depressions 24 (cf. Figures 2, 4 and 16; col. 8, l. 66 – col. 9, l. 5) are to be kept away from the edge areas by a distance 27 at least twice the (finite) thickness of the thickness of the intrinsic region 16 for the specific purpose of enhancing the advantageous characteristics of the diode 10 by causing the device current to be away from the sidewalls and their trap levels, thereby greatly reducing Shockley-Read-Hall charge carrier recombination effects detrimental to the charge that can be stored in the device (cf. col. 2, l. 4-22, col. 2, l. 42-61). *Motivation* to include the teaching by Goodrich et al in the device by Henry et al is the consequent improvement of the amount of charge storable in the PIN diode.

4. ***Claims 9-10 and 12-15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al (FR 75 24147) in view of Rummenik (4,220,963) and Goodrich et al (5,343,070). Henry et al introduce depressions 111 and 112 (cf. page 2, l. 15-21) into a wafer 1/2 (cf. page 2, l. 26-30; see also page 4, l. 5-7) of first conductivity type (N-type); introducing doping atoms to peripheral regions 1 and 3 on both sides of the wafer by carrying out a diffusion process (cf. page 1, l. 30-37), yielding heavily doped peripheral regions 1 and 3 (cf. Figures 2 and 3; cf. page 2, l. 26-30); dicing the wafer into individual chips (cf. page 5, l. 7-10 and Figure 1) so that, in an internal area, each of the chips has at least one depression (cf. Figures 1 and 3), said depression being an essential part of the device; and sawing the depressions (page 1, l. 37 – page 2, l. 3).

Henry et al do not necessarily teach the further limitation that the method with which the doping atoms are introduced to peripheral regions 1 and 3 comprises the steps of coating both sides of the wafer with said doping atoms and carrying out a diffusion process. However, it would have been obvious to include said further limitation in view of Rummenik, who teaches in a patent on a fast recovery diode, hence analogous art, the use of diffusion doping to create desired doped peripheral regions 11 and 12 on opposite sides of the wafer (cf. col. 2, l. 26-38). Motivation to include the method step taught by Rummenik in the method by Henry et al stems from the advantage that many wafers can be simultaneously subjected to diffusion doping through the use of a diffusion furnace. Combination of the teaching by Rummenik with the invention by Henry et al is straightforward through the use of the single heating step described by Rummenik (cf. col. 2, l. 26-38). Success in the implementation of said combination can therefore be reasonably expected.

Henry et al do not necessarily teach the limitation that said depression to be sawed in an internal area such that none of the first layer, second layer and third layer include edge areas that have depressions. *However, it would have been obvious* to include said limitation in view of Goodrich et al, who teach a mesa type PIN diode (cf. title) and a method of making mesa type PIN diodes (cf. abstract) wherein the depressions 24 (cf. Figures 2, 4 and 16; col. 8, l. 66 – col. 9, l. 5) are to be kept away from the edge areas by a distance 27 at least twice the (finite) thickness of the thickness of the intrinsic region 16 for the specific purpose of enhancing the advantageous characteristics of the diode 10 by causing the device current to be away from the

sidewalls and their trap levels, thereby greatly reducing Shockley-Read-Hall charge carrier recombination effects detrimental to the charge that can be stored in the device (cf. col. 2, l. 4-22, col. 2, l. 42-61). *Motivation* to include the teaching by Goodrich et al in the device by Henry et al is the consequent improvement of the amount of charge storable in the PIN diode.

On claim 10: the depressions 111/112 are formed as pits, having rectangular cross sections (cf. Figures 2 and 3).

On claim 12: the wafer according to the method by Henry et al is diced in areas where no depressions have been introduced (cf. page1, l. 37 – col. 2, l. 5).

On claim 13: the method by Henry further comprises the step covering a top side of the wafer using a dopant of second conductivity type (p+ type in Figure 2).

On claim 14: the method by Henry further comprises the step covering a bottom side of the wafer using a dopant of the first conductivity type (n+ type in Figure 2).

On claim 15: Henry et al teach that metal layers may be applied to both layers 1 and 3 (cf. page 3, l. 6-14) (only the metallization of 30 is actually shown, but the metallization of the bottom layer is included in the disclosure through lines 11-14 of page 3).

1. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al, Rummenik and Goodrich et al as applied to claim 9 above, and further in view of Schmid et al (5,985,067), or, in the alternative over Henry et al in view of Rummenik and Goodrich et al as applied to claim 9. Although neither Henry et al nor Rummenik

nor Goodrich et al necessarily disclose the further limitation of claim 11 it is inherent to a PIN diode as taught by Henry et al to have both front and back side metallization as otherwise no electrical utility is feasible; furthermore, with regard to the order of steps implied by the further limitation of claim 11, it would have been obvious to include said further limitation in view of Schmid et al, who, in a patent on a method to produce chips from a metallized wafer (cf. abstract), - hence analogous art, teaches face metallization strips 101-105 on a first main surface 112 of a wafer 100 and face metallization strips 106-110 on a second main surface of said wafer 100 (cf. col. 8, l. 57-61), and a method of cutting the wafer that comprises the step of cutting the wafer 100 along the face metallization strips (cf. claim 5 of Schmid et al; cf. col. 9, l. 27-31; also see end result in Figure 3, with face metallization strips 130 and 131 (cf. col. 9, l. 58-61)).

Motivation to include the teaching by Schmid et al in the invention by Henry et al, Rummenik and Goodrich et al derives from the improved voltage distribution over the metallic components (cf. col. 3, l. 7-18). Combination of said teaching with said invention only requires following the same dicing technique followed by Schmid et al and in no way interferes with the remainder of the invention by Henry et al, Rummenik and Goodrich et al. Success of the implementation of said combination can therefore be reasonably expected.

In the alternative rejection over merely Henry et al, Rummenik and Goodrich et al, Applicant is reminded of Ex Part Rubin, 128 USPQ 440 (Bd. App. 1959) (Prior Art disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to

render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious). Consequently, in view of the absence of any teaching in Applicant's disclosure as to the critical nature of the order in which the metallization and the cutting steps are to be performed the further limitation of claim 11 thus only reduces to the application of metal layers to both sides of the wafer, which is inherent in any PIN diode.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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JPM
February 21, 2004